An electric fuse is known as another program element. For example, USP No. 5,110,754 has described a technology wherein an antifuse corresponding to a kind of electric fuse is used for defective relief or the like of a DRAM. The antifuse has a configuration capable of being programmed by dielectric breakdown of an oxide film held in an insulating state. Further, USP No. 5,742,555 has shown, as an example of an antifuse, an example in which an oxide film is used to form a capacitor in a p-type well region, and a negative voltage is applied to a well electrode of the capacitor and a positive voltage is applied to a plate electrode on the oxide film to thereby bring a gate oxide film into dielectric breakdown. As other references each having described a semiconductor integrated circuit using an electric fuse, there are known USP No. 5,324,681, etc.

IN THE CLAIMS

Cancel claims 10-22, without prejudice or disclaimer, and rewrite claims 1-2, 5, 9 and 23-28, as follows:

1. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a plurality of circuit elements formed in an element forming layer on said semiconductor substrate;

a plurality of first and second terminals formed on the surface of said element forming layer and connected to predetermined ones of said circuit elements;

a plurality of conductive layers which are respectively connected to said first terminals corresponding to some terminals of said plurality of terminals and extending on said element forming layer;

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protruding electrodes respectively connected to said conductive layers;

testing pads respectively connected to said second terminals, said testing pads being not coupled to any protruding electrode; and

an insulating film which covers the surfaces of said protruding electrodes and said testing pads so as to expose said protruding electrodes and said testing pads.

2. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a plurality of circuit elements formed in an element forming layer on said semiconductor substrate;

first and second terminals formed on the surface of said element forming layer and connected to predetermined ones of said circuit elements;

a conductive layer which is connected to said first terminal;

B2

a protruding electrode connected to said conductive layer;

a testing pad connected to said second terminal, said testing pad being not coupled to any protruding electrode; and

an insulating film which covers the surfaces of said protruding electrode and said testing pad so as to expose said protruding electrode and said testing pad.

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5. (Amended) The semiconductor integrated circuit device according to claim 3, wherein said insulating film is a film which contains an organic substance.

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9. (Amended) The semiconductor integrated circuit device according to claim 3, wherein said testing pads extend on said further insulating film.

23. (Amended) A semiconductor integrated circuit device comprising:

B5

a semiconductor substrate;

a first circuit element and a second circuit element formed on said semiconductor substrate;

a wiring formed over said semiconductor substrate and connected to said first circuit element;

a bump formed over said wiring and connected thereto; and

a conductive layer, which is formed over said semiconductor substrate and connected to said second circuit element and which constitutes a testing pad,

wherein said conductive layer is electrically isolated from any bump.

24. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a semiconductor integrated circuit element formed in said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said semiconductor integrated circuit element;

a bump formed on said wiring and connected thereto; and

a conductive layer, which is formed on said semiconductor substrate and connected to said semiconductor integrated circuit element and which constitutes a testing pad which is electrically isolated from any bump,

wherein when said semiconductor integrated circuit element is tested, said testing pad is electrically connected to the outside of said semiconductor integrated circuit device, and

when said semiconductor integrated circuit element is in normal operation, said testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

B5 Cont.

25. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

integrated circuit elements formed on said semiconductor substrate;

a plurality of wirings formed on said semiconductor substrate and connected to said integrated circuit elements;

a plurality of bumps formed on said plurality of wirings and provided in association with said plurality of wirings;

a conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit elements and which is formed as a testing pad which is electrically isolated from any bump; and

an organic film placed on said semiconductor substrate and formed below said plurality of wirings,

wherein when said each integrated circuit element is tested, each said testing pad is electrically connected to the outside of said semiconductor integrated circuit device, and

B5 cont.

when each said integrated circuit element is in normal operation, each said testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

26. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

a first circuit element and a second circuit element formed on said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said first circuit element;

a bump formed on said wiring and connected thereto;

a first conductive material, which is formed on said semiconductor substrate and connected to said first circuit element and which constitutes a first testing pad; and

a second conductive material, which is formed on said semiconductor substrate and connected to said second circuit element and which constitutes a second testing pad which is not connected to any bump,

B5 cont.

wherein when said first circuit element and said second circuit element are tested, said first testing pad and said second testing pad are electrically connected to the outside of said semiconductor integrated circuit device, and

when said first circuit element and said second circuit element are in normal operation, said first testing pad is electrically connected to the outside of said semiconductor integrated circuit device through said bump, and said second testing pad is electrically disconnected from the outside of said semiconductor integrated circuit device.

27. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

an integrated circuit formed on said semiconductor substrate;

a wiring formed on said semiconductor substrate and connected to said integrated circuit;

a bump formed on said wiring and connected thereto;

a first conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit and which constitutes a first testing pad; and

B5 Cont.

a second conductive layer, which is formed on said semiconductor substrate and connected to said integrated circuit and which constitutes a second testing pad which is not connected to any bump,

wherein said first conductive layer and said wiring are connected to each other, and

when said integrated circuit is tested, said first testing pad and said second testing pad are electrically connected to the outside of said semiconductor integrated circuit device and

when said integrated circuit is in normal operation, said first testing pad is electrically connected to the outside of said semiconductor integrated circuit device and said second testing pad is electrically isolated from the outside of said semiconductor integrated circuit device.

28. (Amended) A semiconductor integrated circuit device comprising:

a semiconductor substrate;

integrated circuit elements formed on said semiconductor substrate;

a plurality of wirings formed over said semiconductor substrate and connected to at least one of said integrated circuit elements;

B5 Cont.

a plurality of bumps formed over said plurality of wirings and provided in association with said plurality of wirings;

a conductive layer, which is formed over said semiconductor substrate and connected to at least one of said integrated circuit elements and which constitutes a test pad which is not connected to any bump; and

a film containing an organic material formed between said semiconductor substrate and said plurality of wirings and between said semiconductor substrate and said conductive layer,

wherein when said integrated circuit element is tested, said test pad is electrically connected to the outside of said semiconductor integrated circuit device, and